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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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STEVEN I. WEISBURD
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 AVENUE OF THE AMERICAS
41ST FLOOR
NEW YORK, NY 10036-2714

EXAMINER	
MAYES, MELVIN C	

ART UNIT	PAPER NUMBER
1734	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,180	HARADA ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

(1)

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 18, 2005 has been entered.

Claim Rejections - 35 USC § 112

(2)

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

(3)

Claims 21-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 21 and 23 claim "further comprising arranging the sintered plate on a green sheet, placing another green sheet...and pressing the resulting composite in the direction of lamination." How do these steps relate to the step of Claim 1 of a "providing an unsintered composite laminate comprising a sintered plate...a plurality of green layers..."? Do the "green sheets" correspond to the "green layers" of Claim 1?

Claim Rejections - 35 USC § 103

(4)

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

(5)

Claims 1, 5, 6, 10-12, 16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191.

Gruenwald et al. disclose a method of making a multilayer circuit having incorporated capacitance comprising: providing a structure comprising first and second electrode 1, 2 and either a printed dielectric layer or an already fired ceramic lamina 3 of high dielectric constant (capacitor having a sintered plate); pressing the structure into a green ceramic sheet 11; arranging the structure between green ceramic sheets 11, 13, a green sheet having plated through holes and conductor tracks in contact with the electrodes to form a stack; and firing the green sheets. Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible. As shown in Figure 4, the fired ceramic lamina is of thickness less than the green ceramic sheets so as to be arranged between the green sheets (col. 1, line 31 – col. 2, line 51). Gruenwald et al. do not disclose providing at least one restriction layer on the green sheet laminate.

Mikeska et al. 5,254,191 teach that to reduce XY shrinkage and distortion during firing of a ceramic body such as a multilayer circuit, constraining layers of non-metallic inorganic solids which do not sinter during the sintering of the ceramic body are provided on at least one surface of the unfired ceramic body, and after firing, the porous constraining layer(s) removed from the

sintered ceramic body. Mikeska et al. teach that the use of constraining layers permits the firing of tape layers (green layers) with rigid prefired ceramic substrate while maintaining excellent XY dimensional stability in the layers (col. 2, lines 38-64, col. 4, lines 13-65, col. 13, lines 15-21).).

It would have been obvious to one of ordinary skill in the art to have modified the method of Gruenwald et al. for making a multilayer circuit having incorporated capacitance by providing removable constraining layers which do not sinter on the green sheet laminate, as taught by Mikeska et al, to reduce XY shrinkage and distortion during firing of an unfired multilayer ceramic body (green sheet laminate). Providing constraining layers (restriction layers) on the green sheet stack including the prefired ceramic lamina would have been obvious to one of ordinary skill in the art to reduce XY shrinkage and distortion of the green sheets during the firing of the green sheets to make the multilayer circuit, as Mikeska et al. teach that the use of constraining layers maintains excellent XY dimensional stability of tape layers even when fired with a prefired substrate.

By arranging the capacitor structure having a fired ceramic lamina between stacked green ceramic sheets, as disclosed by Gruenwald et al., an unsintered composite laminate is provided in which a sintered plate of a first ceramic functional material is arranged between primary faces of a pair of adjacent green layers which are in substantially parallel planes, as claimed.

(6)

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claim 5 above, and further in view of Branchevsky 6,252,761.

Branchevsky teaches that since there is a practical limit to the dielectric constant that can be achieved with single layer capacitors, it is desirable to have a multilayer capacitor embedded in a ceramic block to provide increased capacitance compares to single layer capacitors (col. 2, lines 36-51).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the capacitor structure as a multilayer capacitor, as taught by Branchevsky, to provide increased capacitance compared to a single layer capacitor. Providing the capacitor structure as a laminate of fired layers with internal conductor between layers would have been obvious to one of ordinary skill in the art to provide a multilayer capacitor instead of a single layer capacitor, as suggested by Branchevsky.

(7)

Claims 8, 9, 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claims 1 and 12 above, and further in view of JP 6-164150.

Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible.

JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C

and teach that the capacitor can provided to have a dielectric ceramic layer thickness of 12 micrometers (computer translation [0003], [0013]).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the fired dielectric ceramic capacitor lamina of thickness such as 12 micrometers, within the claimed range of 100 micrometer or less, as Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible and JP '150 teaches that dielectric ceramic layer for a capacitor arranged in a ceramic multilayer substrate can be of thickness of 12 micrometers.

It would have been obvious to one of ordinary skill in the art to have further modified the method of the references as combined by providing the green sheets of composition that can be fired in the range of 900-1000°C, as JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C. Providing the green sheets which fire at 900-1000°C as comprised of glass or ceramic and at least 5 weight percent glass, as claimed in Claims 14 and 15, would have been obvious to one of ordinary skill in the art, such as taught by Mikeska et al.

(8)

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claim 1 above, and further in view of either Kodama et al. 5,277,723 or IBM Technical Disclosure Bulletin, February 1978 (entitled "Internal Capacitors and Resistors for Multilayer Ceramic Modules").

Kodama et al. teach that in producing a multilayer ceramic body having capacitors, a plurality of capacitors can be provided to be positioned inside the final laminate (Fig. 19).

IBM Technical Disclosure Bulletin, February 1978 teaches that resistors and capacitors can be built into a MLC substrate by inserting a ceramic disk between greensheets.

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing a plurality of capacitor structures or resistors and capacitors between the green ceramic sheets, as taught by Kodama et al. or IBM Technical Disclosure Bulletin, as known on the art to provide more than one capacitor or combination of capacitor and resistor in a multilayer ceramic body. Providing more than one capacitor or a combination of capacitor and resistor between the green sheets would have been obvious to one of ordinary skill in the art, as suggested by Kodama et al. or IBM Technical Disclosure Bulletin.

(9)

Claims 1, 5, 6, 10-12, 16, 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin, February 1978 (entitled "Internal Capacitors and Resistors for Multilayer Ceramic Modules") in view of Mikeska et al. 5,254,191 or in view of Steinle et al. 5,876,538 and Mikeska et al. 5,254,191.

IBM Technical Disclosure Bulletin discloses a method of making a multilayer ceramic module having resistors and/or capacitors built into the module comprising: inserting a prepared capacitor element between greensheets 12, 14, the capacitor element comprising either a ceramic disk coated with sintered metallurgy 10, a ceramic disk 23 or a layer of dielectric material 25 deposited on one of the greensheets, the greensheets having metallurgy filled vias 18 in contact with the metallurgy of the capacitor element and connecting metallurgy stripes 20; assembling

the greensheets; and sintering. IBM Technical Disclosure Bulletin does not disclose providing at least one restriction layer on the assembled green sheets.

Mikeska et al. 5,254,191 teach that to reduce XY shrinkage and distortion during firing of a ceramic body such as a multilayer circuit, constraining layers of non-metallic inorganic solids which do not sinter during the sintering of the ceramic body are provided on at least one surface of the unfired ceramic body, and after firing, the porous constraining layer(s) removed from the sintered ceramic body. Mikeska et al. teach that the use of constraining layers permits the firing of tape layers (green layers) with rigid prefired ceramic substrate while maintaining excellent XY dimensional stability in the layers (col. 2, lines 38-64, col. 4, lines 13-65, col. 13, lines 15-21).

Steinle et al. teach that a ceramic multilayer substrate is provided with integrated capacitors by providing the capacitor structure on a first green ceramic film; placing another green film thereon and pressing the films together so that the capacitor structure is pressed into the ceramic films (col. 3, line 5 – col. 4, line 10).

It would have been obvious to one of ordinary skill in the art to have modified the method of IBM Technical Disclosure Bulletin for making a multilayer ceramic module having built-in resistors or capacitors by providing removable constraining layers which do not sinter on the assembled greensheets, as taught by Mikeska et al, to reduce XY shrinkage and distortion during firing of an unfired multilayer ceramic body (green sheet laminate). Providing constraining layers (restriction layers) on the assembled greensheet stack including the ceramic disk(s) (prefired ceramic) would have been obvious to one of ordinary skill in the art to reduce XY shrinkage and distortion of the greensheets during the firing of the green sheets to make the

multilayer module, as Mikeska et al. teach that the use of constraining layers maintains excellent XY dimensional stability of tape layers even when fired with a prefired substrate.

By arranging the capacitor element(s) and/or resistor element(s) having a fired ceramic disk between assembled greensheets, as disclosed by IBM Technical Disclosure Bulletin, an unsintered composite laminate is provided in which a sintered plate of a first ceramic functional material is arranged between primary faces of a pair of adjacent green layers which are in substantially parallel planes, as claimed.

Providing the capacitor element between the greensheets by placing the capacitor element on one of the green sheets, placing the other greensheet thereon then pressing, as claimed in Claims 21 and 23, would have been obvious to one of ordinary skill to assemble the capacitor element between greensheets, and further as taught by Steinle et al. as the method steps used to provide a capacitor structure integrated between green sheets for providing a ceramic multilayer substrate is provided with integrated capacitors.

Response to Arguments

(10)

Applicant's arguments filed November 18, 2005 have been fully considered but they are not persuasive.

Applicant argues that Gruenwald prefers using dielectric paste, that there is no suggestion that the ceramics are different and that in Gruenwald, at no time is the dielectric above the surface of green ceramic layer as it must be to meet the requirement of Claim1 that the sintered plate be "between primary faces of a pair of adjacent green layers...which are in substantially

parallel planes." Applicant argues that the present invention places the capacitor element on a green sheet onto which other green sheets are placed. Applicant argues that Mikeska does not suggest using restraining layers with a structure which contains both green and sintered materials.

(11)

It is not required by Claim 1 that the fire plate be above the surface of a green layer or that the plate is placed on a green layer, as argued. It is only required that in the unsintered composite laminate, the sintered plate be "between primary faces of a pair of adjacent green layers...which are in substantially parallel planes." According to Applicants' specification, this appears to be the embodiment as shown in Figures 1-4 where a capacitor is between adjacent green sheets. As shown, the plate is embedded between green sheets in the unsintered laminate. Although as shown, the plate is embedded in the green layer overlying the green layer on which the plate lies, the unsintered composite laminate as claimed encompasses any embodiment where the plate is between adjacent green layers, whether it is embedded into either or both of the adjacent green layers by pressing. Nevertheless IBM Technical Disclosure Bulletin discloses placing a fired ceramic disk between adjacent greensheets.

With respect the Gruenwald, a laminate is formed having a fired capacitor between adjacent green sheets (layers). The laminate formed is essentially no different that that formed by Applicant's embodiment of Figures 1-4 and the capacitor no more forms the surface of a green sheet than Applicant's embedded capacitor forms a surface of a green layer in the unsintered composite laminate in Figures 1-4. Gruenwald does not state that using dielectric paste is preferred. The ceramic of the fired ceramic lamina for the capacitor and the ceramic of the green

sheets are different because Gruenwald disclose using material for the capacitor which cannot be fired with the green sheets and disclose that the ceramic for the capacitor has high dielectric constant, which is not required for ceramic for a multilayer circuit.

As set forth in the rejections, Mikeska et al. teach that the use of constraining layers permits the firing of tape layers (green layers) with rigid prefired ceramic substrate while maintaining excellent XY dimensional stability in the layers. Mikeska et al. thus do suggest using shrinkage restricting layers with a structure which contains both green and sintered materials, which would have suggested to one of ordinary skill in the art to use shrinkage restricting layers to reduce shrinkage of green sheets during firing of a laminate even if there is prefired material as a part of the laminate. The Examiner would also like to point out that JP 10/75060 already of record also teaches using shrinkage restricting layers when making a multilayer substrate containing a capacitor.

Conclusion

(12)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
November 8, 2005